What is claimed is:

1. A method for programming a nitride read only memory cell having a gate input and two source/drain regions, the method comprising:
applying a ramp voltage to the gate input;
applying a constant voltage to one of the two source/drain regions; and
applying a ground potential to the remaining source/drain region.

2. The method of claim 1 wherein the source/drain region to which the constant voltage is applied is acting as a drain region and the source/drain region to which the ground potential is applied is acting as a source region.

3. The method of claim 1 wherein the ramp voltage starts in a range of 0 to 6V and ends in a range of 4 to 12V.

4. The method of claim 1 wherein the ramp voltage has a time period in a range of 1 microsecond to 1 millisecond from start to end.

5. The method of claim 1 wherein the ramp voltage starts at 5V and goes to 10V.

6. The method of claim 1 wherein the constant voltage is in a range of 3.5 to 6V.

7. The method of claim 1 wherein the nitride read only memory cell is embedded in a CMOS device.

8. A nitride read only memory (NROM) cell embedded in a CMOS device, the NROM cell comprising:
a gate input coupled to a ramp voltage;
a first source/drain region coupled to a constant voltage; and
a second source/drain region coupled to a ground potential.

9. The NROM cell of claim 8 and further comprising an oxide-nitride-oxide region between the first and second source/drain regions that can hold a data bit on each end of the oxide-nitride-oxide region.

10. The NROM cell of claim 8 and further comprising an oxide-nitride-oxide region between the first and second source/drain regions that can hold a single data bit.

11. The NROM cell of claim 8 wherein the constant voltage is in a range of 3.5 to 6V and the ramp voltage starts in a range of 0 to 6V and ends in a range of 4 to 12V over a time period in a range of 1 microsecond to 1 millisecond.

12. A method for performing an erase operation on a nitride read only memory cell having a gate input and two source/drain regions, the method comprising:
applying a constant voltage to the gate input;
applying a constant positive current into a first of the source/drain regions; and
allowing the remaining source/drain region to float.

13. The method of claim 12 wherein the nitride memory cell is embedded in a CMOS device.

14. The method of claim 12 wherein the constant gate voltage is in a range of 0 to – 12V.

15. The method of claim 12 wherein the constant positive current is in a range of 0.1nA to 10 μA per cell.

16. The method of claim 12 wherein the erase operation has a duration in a range of 1 μs to 1 second.

17. The method of claim 12 and further including:
monitoring the first source/drain region for a predetermined voltage level; and
ending the erase operation when the predetermined voltage level is reached.

18. A method for erasing a nitride read only memory cell having a gate input and two source/drain regions, the method comprising:
applying a constant voltage to the gate input;
applying a constant positive current into a first of the source/drain regions; and
applying a ground potential to the remaining source/drain region.

19. The method of claim 18 and further including:
monitoring the first source/drain region for a predetermined voltage level; and
ending the erase operation when the predetermined voltage level is reached.

20. The method of claim 18 wherein the constant gate voltage is in a range of 0 to –12V, the constant positive current is in a range of 0.1nA to 10 μA per cell, and the erase operation has a duration in a range of 1 μs to 1 second.

21. A method for erasing a nitride read only memory cell having a gate input and two source/drain regions, the method comprising:
applying a constant voltage to the gate input;
applying a constant positive current into a first source/drain region; and
coupling the remaining source/drain region to the first source/drain region.

22. The method of claim 21 wherein constant gate voltage is in a range of 0 to –12V, the constant positive current is in a range of 0.1nA to 10 μA per cell, and the erase operation has a duration in a range of 1 μs to 1 second.

23. The method of claim 21 and further including:
monitoring the first source/drain region for a predetermined voltage level; and

ending the erase operation when the predetermined voltage level is reached.

24. A method for erasing a nitride read only memory cell having a gate input and two source/drain regions, the method comprising:
applying a constant voltage to a first of the source/drain regions;
applying a negatively ramped voltage to the gate input; and
allowing the remaining source/drain region to float.

25. The method of claim 24 wherein the constant voltage is in a range of 3.5 to 6V and the negatively ramped voltage starts in a range of 0 to -7V and ends in a range of -4 to -12V over a time period in a range of 1 microsecond to 1 millisecond.

26. A method for erasing a nitride read only memory cell having a gate input and two source/drain regions, the method comprising:
applying a constant voltage to a first of the source/drain regions;
applying a negatively ramped voltage to the gate input; and
coupling the remaining source/drain region to the first source/drain region.

27. A method for erasing a nitride read only memory cell having a gate input and two source/drain regions, the method comprising:
applying a constant voltage to a first of the source/drain regions;
applying a negatively ramped voltage to the gate input; and
applying a ground potential to the remaining source/drain region.